Reduction of Common Mode Voltage and Conducted EMI Through Three Phase Inverter Topology

Casey T. Morris, Di Han, Bulent Sarlioglu, *Senior Member, IEEE*
Wisconsin Electric Machines and Power Electronics Consortium (WEMPEC)
University of Wisconsin-Madison
Madison, WI 53706 USA

Corresponding author:
Prof. Bulent Sarlioglu
807 Extension Building
432 North Lake Street
Madison, WI 53706
Ph: (608) 262-2703
Fax: (608) 263-3160
sarlioglu@wisc.edu

(This manuscript has not been been submitted previously and is intended to be submitted for review as a Letter.)

Abstract—**This letter presents a three phase voltage source inverter (VSI) topology to reduce the common mode (CM) voltage and electromagnetic interference (EMI) of electric motor drives. Instead of using filters, active or passive, or specific PWM techniques to reduce the CM voltage, the proposed topology has inherently less CM voltage generation. Like some CM reducing PWM methods that aim to eliminate the use of the zero state vectors of the inverter to reduce the CM voltage, this topology effectively eliminates these zero states through the addition of two switches placed in series on the DC lines that act to "float" the inverter from the DC source during times of the zero states. This has the same effect on the CM voltage as the PWM techniques; however, this topology can be implemented with any PWM method and does not add any additional complexity to standard control techniques. The operation and CM reduction capability of the topology is first demonstrated in simulation and then verified with experimental results. A comparison of both common mode voltage and EMI is made to a conventional three phase VSI to demonstrate the effectiveness of proposed topology.**

***Index Terms*— Common mode EMI, common mode voltage, EMI mitigation, inverter topology.**

I. Introduction

Common mode (CM) voltage is a major area of interest in applications such as electric motor drives. These voltages produced by standard pulse width modulated (PWM) inverters have long been known to cause a variety of problems, from electromagnetic interference (EMI) emissions [1] to bearing currents. These bearing currents induced by the CM voltage are of particular significance as they can negatively affect the lifetime and reliability of a machine [2]. CM voltages and currents also cause problems for motor drive designers as they are hard to model with accuracy and as a result, designing optimal mitigation methods is difficult.

The literature is full of research regarding methods of mitigating the CM voltages and currents. Some of the most popular CM voltage reduction techniques include filters, both passive [3] and active [4]. Passive filters utilize inductors and capacitors to attenuate the high frequency components of the voltages and currents. Instead of mismatching the impedances, reference [5] proposed an impedance balancing method to reduce the CM voltage. Active filters, on the other hand, typically use controllable devices to produce currents to cancel the CM currents created by the CM voltages. A variety of filter topologies and design methods have been proposed to mitigate CM voltage and EMI [6]–[9]; however, these techniques often have drawbacks of being bulky or complex.

Alternative methods to reduce the CM voltage have been proposed in the form of PWM techniques. To understand how these are effective, it is important to understand the CM voltage of a three phase voltage source inverter (VSI) as (1).

$$V_{cm} = \frac{1}{3}\left(V_a + V_b + V_c\right) \tag{1}$$

From (1), V_{cm} can be calculated for each of the eight inverter states, and is found to be +/- $V_{dc}/6$ for the six active states and +/- $V_{dc}/2$ for the two zero states [10]. The CM reducing PWM techniques, near state PWM (NSPWM) and active zero state PWM (AZSPWM), thus, propose algorithms that do not use the zero states. As described in [11], AZSPWM uses two states that are 180° apart to synthesize a time averaged zero vector. Alternatively, NSPWM uses three of the active states to synthesize the commanded waveform [12]. While these are able to reduce the CM voltage, they have limitations, such as the bipolar line-to-line voltages that can cause overvoltage at high modulation indices and increased output current THD with AZSPWM, or the voltage linearity issue of NSPWM that prevents it from synthesizing low modulation index voltages [13].

In addition, much research has focused on various inverter topologies that aim to inherently reduce the CM voltage. In reference [14], the H5 topology adds a switch in series between the DC source and the inverter; however, this is used in a single-phase full bridge inverter and the underlying operating paradigm (freewheeling current paths) and switching methodology cannot be directly extended to a three phase application. Similarly, the full bridge "Heric" topology adds two switches at the output of the inverter in parallel with the load to operate in the zero states with minimal CM voltage

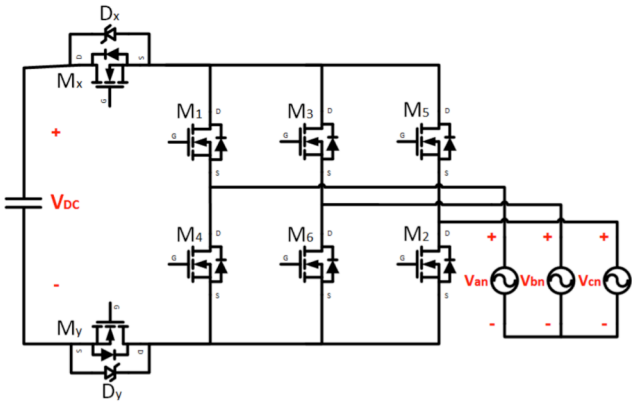

Fig. 1. Proposed inverter topology with extra switches between phase legs and DC capacitors.

[15]. Additionally, other single phase full bridge inverters have been proposed to reduce CM voltage, typically for transformerless solar applications [16]. However, there is a knowledge gap pertaining to three-phase inverter topologies to reduce CM voltage, which enable uses in automotive and industrial applications.

This paper proposes a three phase VSI topology that builds on the concepts and capabilities of existing single phase topologies and has the same effect of CM reducing PWM techniques without their limitations. In addition, this topology also enables the capability to utilize other PWM techniques that have been optimized for various factors. The proposed topology has benefits such as reduced CM voltage without added complexity and it can be implemented with conventional control and PWM techniques. The proposed method is compared with a conventional VSI in terms of CM voltage and EMI reduction, showing significant improvement.

II. Proposed Inverter Theory

The main goal of the proposed inverter, shown in Fig. 1, is to reduce the CM voltage during the zero states of the PWM technique. Instead of developing an alternative PWM technique, the knowledge of the zero states is utilized.

A. Operating Principles

While it has been shown that the zero states have the maximum amount of CM voltage, it is worthwhile to remember that the point of these zero states is to provide three 0 V line to line voltages. The problem with the CM voltage is that all of the phases are tied to the same maximum magnitude voltage to create these 0 V line to line voltages. The proposed topology solves this problem by adding two switches connecting the DC bus to the inverter input, as shown in Fig. 1. These switches are closed, or conducting, at all times except when all three phase legs are tied to the same DC line. At this point, the extra switch, M_x or M_y, is opened, disconnecting the inverter from the DC source. Thus, the 0 V line to line voltages are provided to the motor; however, the input terminals of the inverter are "floated" and can be pulled to zero through the parasitic capacitances associated with the machine. This theoretical waveform is shown as the red solid

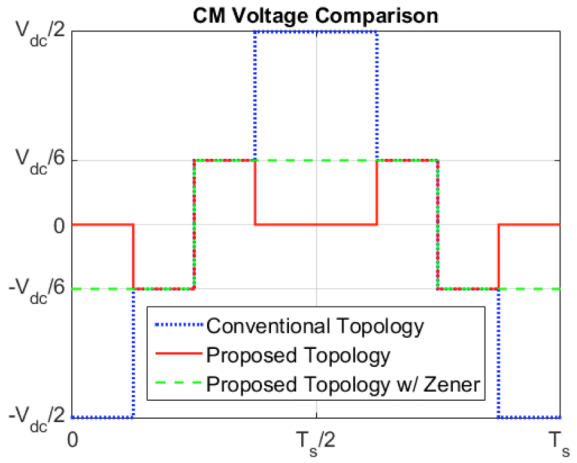

Fig. 2. Common mode voltage of conventional inverter compared to proposed inverter.

line in Fig. 2 compared to the conventional blue dotted waveform.

In Fig. 2, the sequence of states is shown for an example sampling period of SVPWM when the command voltage vector is between states 1 and 2. Also, in this example, the time in all states is assumed the same; however, in many cases, the time in states 0 and 7 can be much less than the other states, except at low modulation indices.

Due to many of the parasitics in the system, such as the output capacitances of the switches, it is not always practical to achieve exactly a 0 V during the floated zero states. The actual voltage may vary widely for a variety of factors. For this reason, the anti-parallel Zener diodes, D_x and D_y, may be placed in parallel with the extra switch. The purpose of these is to ensure a consistent CM voltage waveform with less variation and uncertainty in the zero states. If the breakdown voltage of the Zener diodes is chosen as one third of the maximum DC voltage of the variable speed drive, the resulting CM voltage will ideally have at worst the shape of the green dashed line in Fig. 2.

The green dashed line is the same CM voltage waveform that is produced using either the NSPWM or AZSPWM

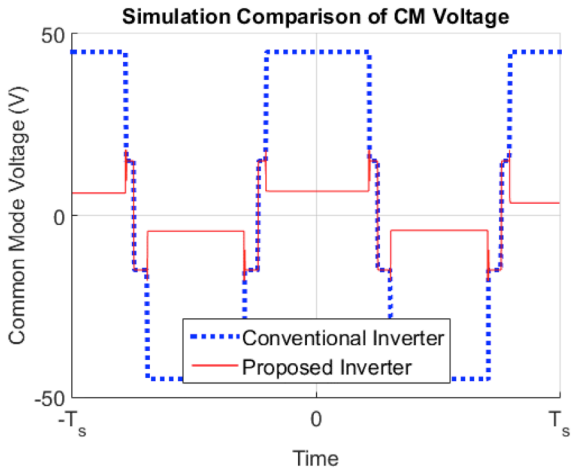

Fig. 3. Simulation of common mode voltage of conventional inverter compared to proposed inverter.

TABLE I
SPECIFICATIONS OF SIMULATION AND EXPERIMENT TEST

Operating Specs.		
Name	Value	Unit
$\mathbf{V_{bus}}$	90	V
$\mathbf{f_s}$	20	kHz
$\mathbf{C_{dc}}$	40	µF
Modulation index	0.2	

technique; however, the limitations of voltage linearity and bipolar line to line voltages are avoided.

III. SIMULATION RESULTS

The proposed inverter is realized in LTSpice simulation software to verify the operation principles. The results are compared to a conventional inverter, i.e. the extra switches are replaced with short circuits.

A. Simulation Model

To simulate the proposed inverter, a motor drive system is modeled and sine PWM is used to modulate the phase legs. In addition to the inverter and DC source shown in Fig. 1, an induction machine model is added as the load. Si MOSFETs are used to model the switches. With this set up, the CM voltages as described in (1) are calculated. To compare this to the conventional inverter with six switches using sine PWM, all simulations are repeated, with M_x and M_y replaced with short circuits, which serves as the baseline. The specifications of the parameters of the simulation are shown in TABLE I, and no anti-parallel Zener diodes are used.

B. Common Mode Waveforms

The purpose to the simulation is to ensure that the proposed inverter topology has a CM voltage waveform as predicted in Fig. 2. The results of the simulations are shown in Fig. 3, which compares the performance of a conventional three phase inverter utilizing sine PWM to that of the proposed inverter.

As can be seen in Fig. 3, the CM voltage of the proposed inverter is predicted to behave as described earlier. When the conventional inverter goes to a maximum CM voltage of magnitude 45 V, the proposed inverter instead is reduced by 40 V to 5 V. There are some small spikes at the edges of these points, mainly caused by the charging and discharging of the output capacitors of the switches. This is investigated further in the experimental results. The reduction of the 40 V is a result of the extra switch, either M_x or M_y, blocking the rest of the voltage. When the blocking voltage of the extra switch is added to the CM voltage of the floating inverter, it will be identical to the CM voltage of the conventional inverter. This is verified in the experiments.

TABLE II
LOSS AND EFFICIENCY COMPARISON

Operating Specs.		
Name	Conventional	Proposed
M_1 -- M_6 Loss	0.48 W	0.48 W
M_X & M_Y Loss	0 W	0.13 W
Total Loss	0.48 W	0.61 W
Efficiency	98.38%	98.00%

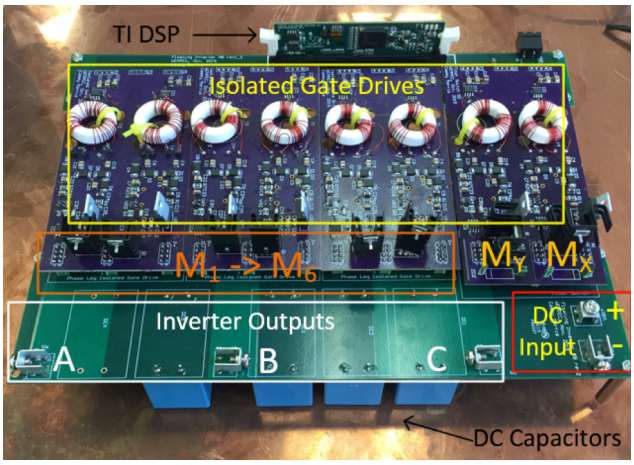

Fig. 4. Realization of the proposed inverter, created in a modular fashion, with key components labeled, photographed on top of copper ground plane.

C. Loss and Efficiency

It is also important to understand the impact on efficiency that the introduction of the extra switches has compared to the conventional inverter. A preliminary loss breakdown and efficiency comparison is shown in Table II. As shown, the efficiency drop relative to the switching and conduction loss of the switches is around 1% at these operating condition. However, this does not consider other loss mechanisms in the converter, namely, the filter. With reduced CM emissions, a reduction or elimination in EMI filter size can be assumed, which in turn reduces the loss associated with the filter. Depending on the conditions, the savings in filter loss may offset the extra switch losses, potentially increasing overall efficiency, and this tradeoff is a topic for further exploration.

IV. EXPERIMENTAL RESULTS

A. Test Setup

A modular version of the proposed inverter is fabricated and the result is shown in Fig. 4. As can be seen, there are four daughter boards (purple) representing the three phase legs and the extra switches. These then plug into the motherboard (green) which provides power to the DSP and the gate drives, and also contains the inputs/outputs and capacitors. To test a conventional inverter, the daughter board with M_x and M_y can be removed and replaced with short circuits to connect the inverter phases to the DC input. A design like this allows the tests to maintain consistency in terms of parasitic capacitances

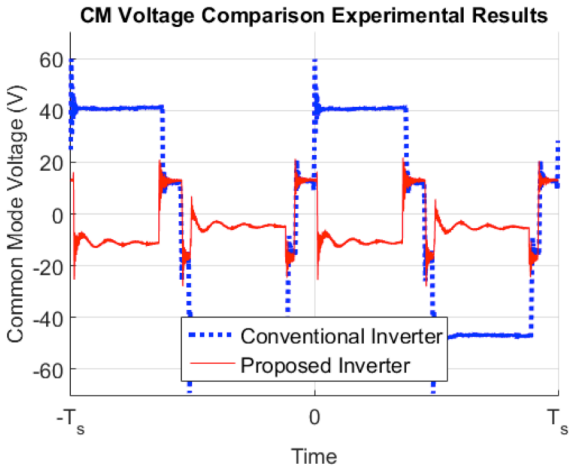

Fig. 5. Experimental measurements of CM voltage of a conventional sine PWM inverter and proposed inverter.

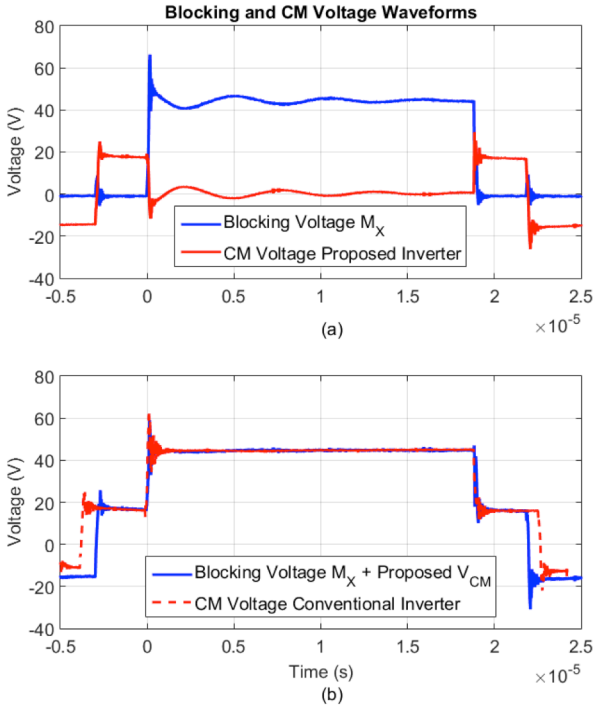

Fig. 6. (a) Blocking voltage of the proposed topology, blocking the DC bus during the zero state allowing for the reduction. (b) Sum of the blocking voltage and CM voltage of proposed inverter compared to conventional inverter CM voltage.

and inductances, allowing for a fair comparison between the two inverters.

Lastly, it is important to note that referencing the gate signals of all of the switches in the proposed inverter is more of a challenge than a conventional inverter. This is due to the fact that the bottom three switches, M_2, M_4, and M_6 are floating relative to the negative of the DC bus. While many solutions exist, individual isolated gate drives are used in this realization for each switch to ensure the proper V_{gs} and to provide symmetry.

An EMI test bench is created with a large grounded copper plane. The DC voltage is connected to the inverter through two line impedance stabilization networks (LISNs), whose

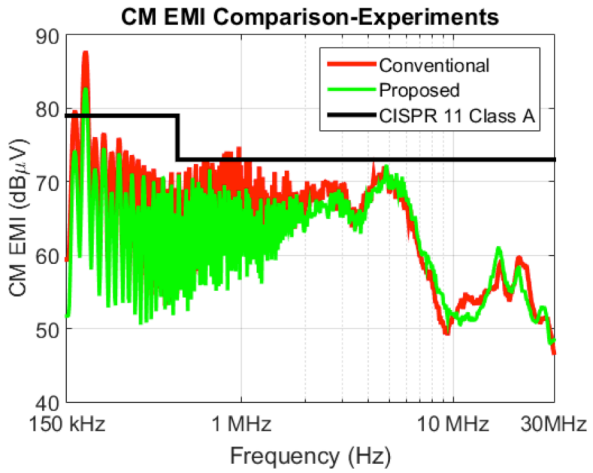

Fig. 7. Experimental measurements of CM EMI of conventional six switch sine PWM inverter and proposed inverter.

midpoint is connected to the ground plane. The inverter outputs are connected to a three phase, ¼ hp, 1725 rpm induction motor, which is unloaded and allowed to spin freely. The specifications of the test are the same as the simulation, as described in TABLE I.

B. Measured Waveforms

The inverter output terminal voltages are measured with a LeCroy Wavesurfer oscilloscope and the CM voltage is computed, as in (1), for both the conventional (six switch topology utilizing sine PWM) and proposed inverter. Additionally, the V_{DS} of M_x (its blocking voltage) is also measured. The CM EMI frequency results are also measured on the two LISNs with a noise separator and recorded with a Rigol spectrum analyzer. These results and comparisons are shown in Figs. 5, 6, and 7.

V. Discussion

A. Common Mode Voltage

As shown in the experimental results, the proposed inverter operates as expected with the predicted CM voltage waveforms. When the conventional inverter experiences a maximum magnitude of 45 V ($V_{dc}/2$), the proposed inverter is shown to have a near zero voltage in Fig. 5 during zero states. Just as the simulations, there are a few small spikes in CM voltage of the proposed inverter, although the spikes are less than that of the conventional inverter, with about a 40 V, or 67%, reduction in peak voltage. The peaks on these transitions from the zero states to the non-zero states and the zero state voltage level are greatly impacted by the gate timing of the extra switches and proper timing can be achieved by manipulating the PWM wave generation of the extra switches.

B. Timing Considerations

In its simplest form, the timing of the extra switch pulses is the NAND of adjacent three switches (for M_x: M_1, M_3, and M_5). Equivalently, if implemented in software, it is the complement of the minimum duty cycle of the adjacent switches. Unfortunately, due to the non-ideal turn on and off characteristics of the switches, it is not quite as simple, and further timing considerations are needed to ensure that the CM voltage is reduced throughout the whole zero state.

Consider the case when the inverter is in an active state, with Phase A tied to the low side and Phases B and C tied to the high side of the DC bus. In this case, M_x and M_4 are on and M_1 is off. When the inverter moves to the zero state, M_x and M_4 will turn off and M_1 will turn on. If M_1 turns on before M_x turns off, the inverter will momentarily be in the conventional zero state. As a result, the output capacitance of M_4 will begin to charge, and as it does, the CM voltage will begin to rise to $V_{dc}/2$. Then, when M_x finally turns off, the output capacitances will be charged and there will be no voltage for M_x to block and no difference will be observed. Thus, it is crucial that the PWM generation account for this phenomena and ensure that M_x is off before M_1 turns on. Similarly, the amount of "dead time" between M_x and M_1 impacts the zero state CM voltage, as it is proportional to the amount of charge across (blocking voltage of) the output capacitors of the off devices.

Similarly timing is crucial at the end of a zero state, as M_x will turn on and M_1 will turn off. However, if M_x turns on and begins conducting before M_1 turns off, all phases will be momentarily tied to the high side of the DC bus, and this can lead to a spike to $V_{dc}/2$ at the end of the zero state. Thus, the PWM generation must account for this time difference to prevent these issues.

The blocking voltage of the extra switch, M_x, is shown in Fig. 6 (a) with the CM voltage. It can be seen that the blocking voltage is 0 V when the inverter is in the non-zero states and the switch is closed. However, when the zero state occurs and the switch is opened, M_x blocks roughly half of the DC bus (dependent on the timing as previously mentioned), allowing the voltage reduction in the CM waveform. When these two waveforms are added together, as in Fig. 6 (b), it is equivalent to the CM voltage of the conventional inverter. This result is as expected and verifies the operating principle of the proposed topology.

C. Common Mode EMI

The EMI noise of the inverter is also of great interest. The reduction in the CM EMI is shown in Fig. 7, which also shows an example EMI standard, CISPR 11 Class A. As can be seen, in the range of 150 kHz to 2 MHz, the proposed inverter has about 5 dB of attenuation, which in this case, almost allows it to pass the EMI standard. In the range above 2 MHz, there is little difference between the conventional and proposed inverter as a result of the parasitics.

The reduction of the CM voltage and EMI demonstrated in these experimental results is of significant consequence. Apart from the EMI reduction in this example enabling the inverter to pass the qualifications with less required attenuation, the reduction in the CM voltage waveform positively impacts the entire motor drive system. The peak to peak is significantly reduced, as is the overall energy in the waveform.

To understand why the CM EMI is reduced, it is important to consider a CM EMI model for the system as shown in Fig.

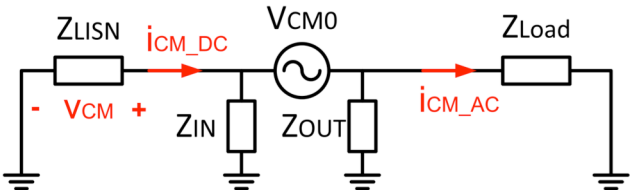

Fig. 8. Model of CM EMI noise coupling path. Both the conventional and proposed inverters have the same impedance values, with only the voltage source different.

8. As mentioned, both the proposed and conventional inverters have the same noise coupling path due to the PCB design; however, they have different CM voltage noise sources, V_{CM0}. Thus, because the proposed inverter reduces the equivalent V_{CM0} (Fig. 5), it follows that the CM EMI is also reduced.

As the bearing current induced in the machine is related to the CM voltage, reducing the CM voltage reduces the bearing current, which can increase the lifetime and reliability of the machine [17].

VI. Conclusion

This letter has proposed a three phase inverter topology for the reduction of the CM voltage, and subsequently the CM EMI. Like previous single phase topologies in literature, the addition of the auxiliary switches enables the phase legs of the inverter to be "floated" from the DC bus, eliminating the high CM voltage problem of the PWM zero states. In comparison to CM reducing PWM algorithms, the proposed topology has the advantages of less computational complexity, unipolar line to line voltages, and complete voltage linearity. While this letter has presented the topology in terms of a motor drive, it is applicable to other types of three phase loads, such as a grid-connected inverter. Continued development is needed with respect to various implementation strategies, such as gate referencing, in order to compete with conventional inverters in terms of energy and power density. However, the improvements in CM voltage and EMI warrant further investigation into the topology.

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